REMARKS

The present Amendment amends claims 17 and 19 and cancels claims 16 and 18. Therefore, the present application has pending claims 17 and 19.

Claims 18 and 19 stand rejected under 35 USC §102(e) as being anticipated by Barrientos (U.S. Patent No. 5,910,899); and claims 16 and 17 stand rejected under 35 USC §103(a) as being unpatentable Barrientos in view of Ramachandran (U.S. Patent No. 6,002,857). As indicated above claims 16 and 18 were canceled. Therefore, these rejections with respect to claims 16 and 18 are rendered moot. These rejections with respect to the remaining claims 17 and 19 are traversed for the following reasons. Applicants submit that the features of the present invention as now recited in claims 17 and 19 are not taught or suggested by Barrientos or Ramachandran whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to each of claims 17 and 19 so as to more clearly describe that the present invention is directed to an information processing system including an input unit for receiving from external of the information processing system, circuit information of a module constituting a semi-conductor integrated circuit, a floorplan which is allocation information of blocks constituting the module and evaluation indices generated based on the circuit information of the module for evaluating modification of the floorplan, wherein the circuit information floorplan and evaluation indices are associated with each other, a storing unit for storing the associated circuit information, floorplan and evaluation indices, and a processing unit

for reading the floorplan stored in the storing unit according to specification information for modifying the floorplan when the specification information is input, generating a plurality of floorplan candidates each being modified based on the read floorplan and the specification information, evaluating the generated floorplan candidates based on the evaluation indices stored in the storing unit and selecting one floorplan based on an evaluation result.

Unique according to the present invention is that the evaluation indices include know-how of a designer who designs a semiconductor integrated circuit to be used in evaluating a generated floorplan.

The above described features of the present invention regarding the know-how of an integrated circuit designer is illustrated, for example, in the Table as set forth in Fig. 19A wherein, for example, block movement and block allocation rules are provided with along with peripheral circuit interface information. The above identified know-how information is recorded as design information so as to be easily used, for example, by a tool which calculates evaluation values, for example, as shown in Fig. 9C of the present application regarding changes being made to the floorplan. These calculated evaluation values are used to improve the quality of the floorplan and create an environment in which the quality of the floorplan would not so closely depend upon the experience or lack thereof of a floorplan designer. Such features are clearly not taught or suggested by any of the references of record particularly Barrientos and Ramachandran whether taken individually or in combination with each other as suggested by the Examiner.

Barrientos teaches, for example, in col. 22, lines 33-41 that:

> "by performing the method described in Fig. 19, the present invention advantageously displays a histogram containing multi-dimensional timing quality feedback information to a floorplan designer enabling the floorplan designer to relate the timing information displayed in the histogram to a graphical view of the paths and/or next selected by the designer, thus enabling the designer to employ his or her expertise knowledge in making intuitive evaluations of the timings quality of the selected floorplan".

In the Office Action, the Examiner refers to the above noted passage of Barrientos as support for the allegation that Barrientos teaches that the evaluation indices include know-how of a designer who designs a semiconductor integrated circuit. However, the Examiner is completely in error in this regard and has mis-described this passage of Barrientos.

In the above noted passage of Barrientos histogram information related to timing information is fedback to a floorplan designer thus enabling the floorplan designer (i.e., human) to employ his or her expert knowledge in making intuitive evaluation of the floorplan based on viewing the timing information. Thus, the problem which is readily apparent in Barrientos is that the result of the floorplan closely depends on the expert knowledge or the lack thereof of the floorplan designer operating the system when viewing the timing information. Thus, by use of the system taught by Barrientos it is highly likely that a less experienced floorplan designer would produce a low quality floorplan due to a mis-interpretation of the timing information.

Another problem which is evident in Barrientos is that only the timing information is fedback to the floorplan designer. Thus, Barrientos fails to teach or suggest the feedback of information other than timing information which can be used by the floorplan designer to design a high quality floorplan. Accordingly, by using the system taught by Barrientos, a floorplan designer would have to read out other information that may be of concern with respect to a target circuit based solely on the floorplan designers' interpretation of the timing information. This places a floorplan designer at a distinct disadvantage in his attempt to develop a high quality floorplan.

The above described deficiencies of Barrientos are overcome by the present invention as clearly recited in the claims. Each of the claims clearly recites that the evaluation indices include know-how of a designer who designs a semiconductor integrated circuit to be used in evaluating a generated floorplan. Such know-how being resident in the evaluation indices is not taught or suggested by Barrientos.

Therefore, Barrientos fails to teach or suggest that the evaluation indices include know-how of a designer who designs a semiconductor integrated circuit to be used in evaluating a generated floorplan as recited in the claims.

Accordingly, reconsideration and withdrawal of the 35 USC §102(e) rejection of claim 19 as being anticipated by Barrientos is respectfully requested.

The above noted deficiencies of Barrientos relative to the features of the present invention now more clearly recited are not supplied by any of the other references of record particularly Ramachandran. Therefore, combining the teachings of Barrientos and Ramachandran still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

Ramachandran, the same as Barrientos, fails to teach or suggest evaluation indices which include know-how of a designer who designs a semiconductor integrated circuit to be used in evaluating a generated floorplan and using such evaluation indices to evaluate a generated floorplan as in the present invention.

Thus, the combination of Barrientos and Ramachandran still fails to teach or suggest the features of the present invention as now more clearly recited in the claims. Therefore, reconsideration and withdrawal of the 35 USC §103(a) rejection of claim 17 as being unpatentable over Barrientos and Ramachandran is respectfully requested.

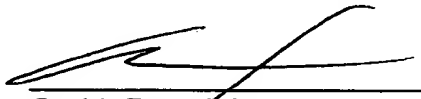
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 16-19.

In view of the foregoing amendments and remarks, Applicants submit that claims 17 and 19 are in condition for allowance. Accordingly, early allowance of claims 17 and 19 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.38174X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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